(12) UK Patent Application (19) GB (11) 2 332 294 (13) A

(43) Date of A Publication 16.06.1999

(21) Application No 9726087.1

(22) Date of Filing 11.12.1997

(51) INT CL[6]
G02F 1/1347 , G09G 3/36

(52) UK CL (Edition Q)
G5C CA310 CA342 CA375

(56) Documents Cited
GB 2062927 A WO 97/32296 A1 US 5164853 A

(58) Field of Search
UK CL (Edition P) G5C CHB
INT CL[6] G02F 1/1347 , G09G 3/36
ONLINE:WPI,INSPEC,JAPIO

(71) Applicant(s)
Sharp Kabushiki Kaisha
(Incorporated in Japan)
22-22 Nagaike-cho, Abeno-ku, Osaka 545-8522, Japan

(72) Inventor(s)
Henning Molsen
Martin David Tillin
Emma Beynon

(74) Agent and/or Address for Service
Marks & Clerk
4220 Nash Court, Oxford Business Park South,
OXFORD, OX4 2RU, United Kingdom

(54) Abstract Title
Multilayer display panels

(57) A double layer colour guest-host active matrix crystal display (GH-AMLCD) comprises a top active matrix substrate 20, a bottom active matrix substrate 30 and a conducting divider 21 interposed between the top and bottom substrates 20, 30. A common scan line driver circuit 43 is provided for applying scan voltages to the substrates 20, 30 by way of scan lines 42, and a common data line driver circuit 45 is provided for applying data voltages to the substrates 20, 30 by way of data lines 44. The 2 N scan lines 42 and the 2 x 3 M data lines 44 are connected to anisotropic conductors 46 and 47 mounted on the bottom substrate 20 and extending along two mutually perpendicular edges of the substrate 30. The N scan lines of the top substrate 20 are connected by the conductor 46 to the N scan lines of the bottom substrate 30 and the 3 M data lines of the top substrate 20 are connected by the conductor 47 to the 3 M data lines of the bottom substrate 30. Such an arrangement enables the number of interconnections from the scan line and data line driver circuitry to the panel to be decreased as compared with a conventional arrangement.

In an alternative (Figure 24) only the data line driver is common to the top and bottom matrix substrates.

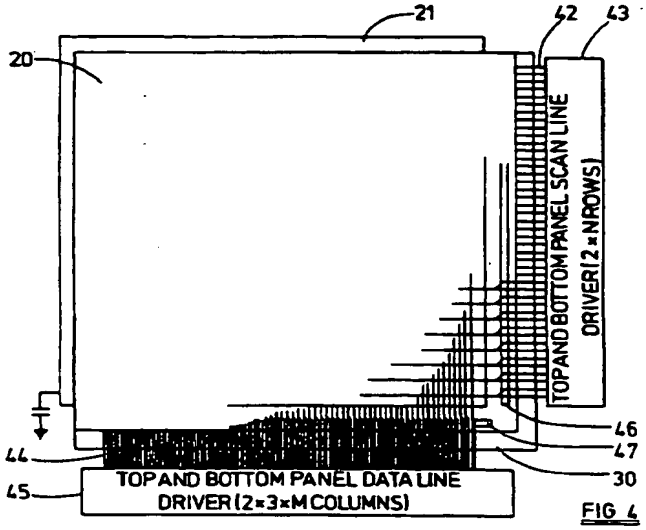

FIG 4

GB 2 332 294 A

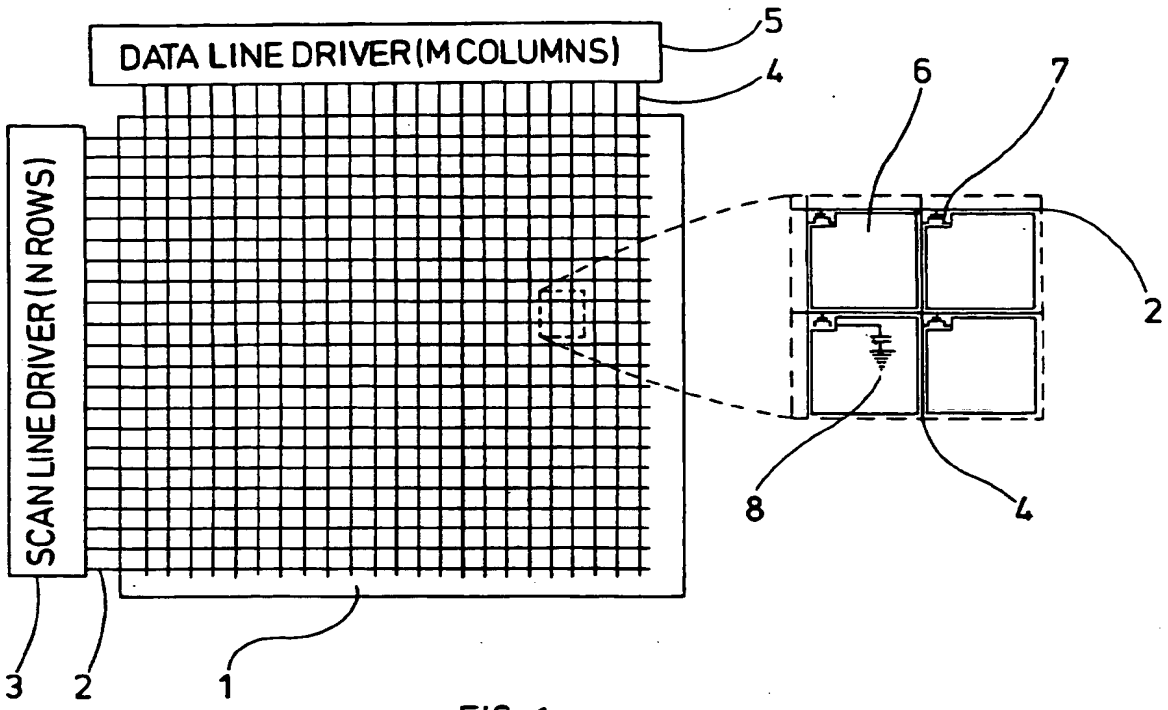
DATA LINE DRIVER (M COLUMNS)
SCAN LINE DRIVER (N ROWS)
5
4
6
7
2
8
4
3
2
1

FIG 1

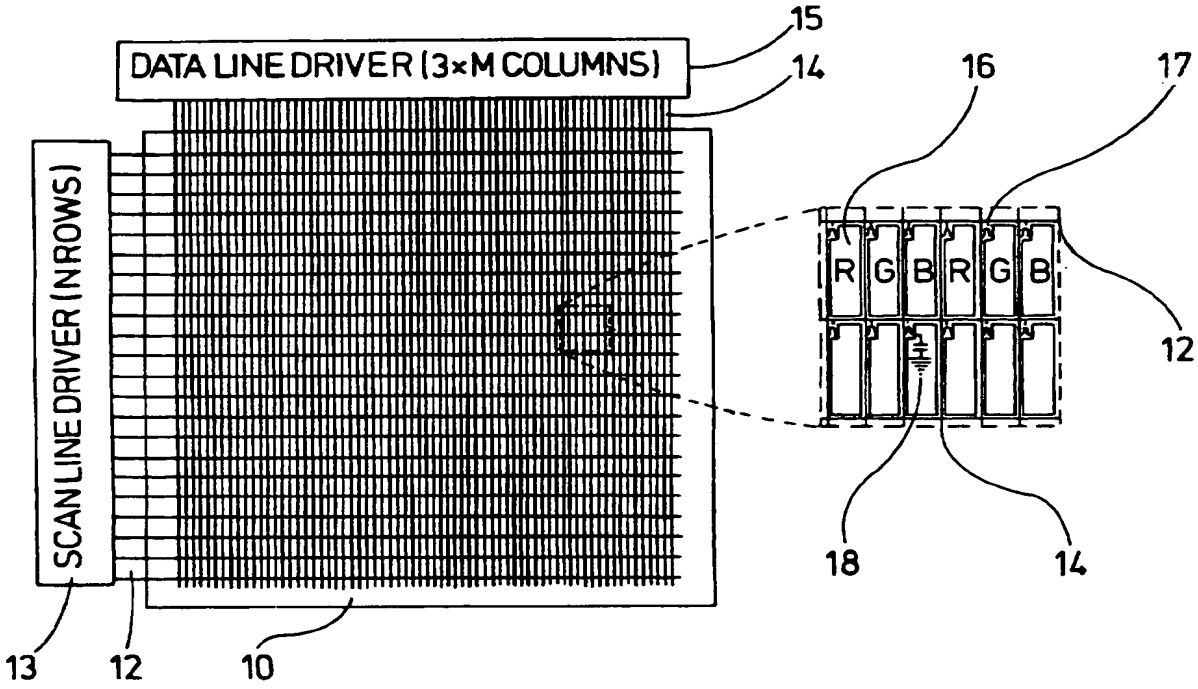
DATA LINE DRIVER (3×M COLUMNS)
SCAN LINE DRIVER (N ROWS)
15
14
16
17
R G B R G B
12
18
14
13
12
10

FIG 2

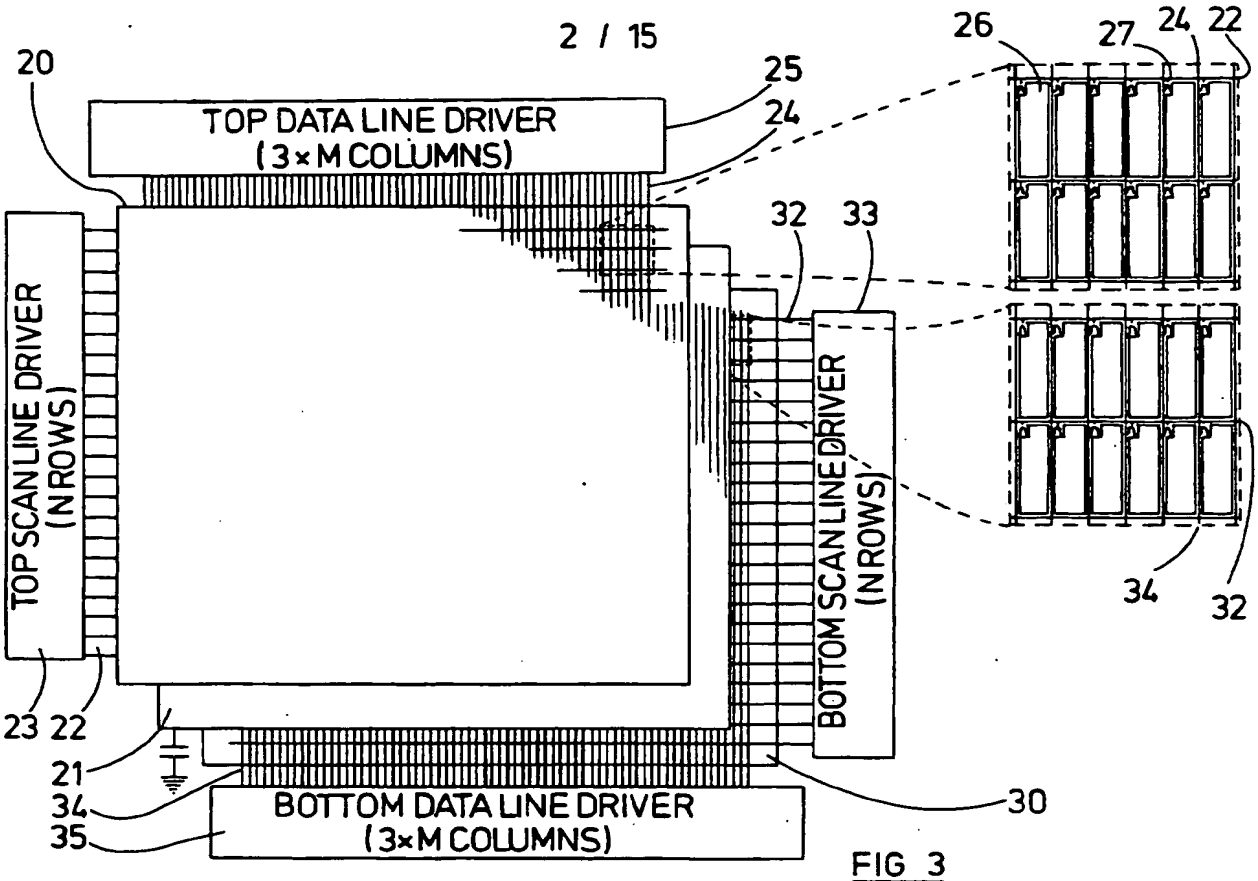
20
TOP DATA LINE DRIVER
(3×M COLUMNS)
25
24
26
27
24
22
32
33
TOP SCAN LINE DRIVER
(N ROWS)
BOTTOM SCAN LINE DRIVER
(N ROWS)
34
32
23
22
21
34
35
BOTTOM DATA LINE DRIVER
(3×M COLUMNS)
30

FIG 3

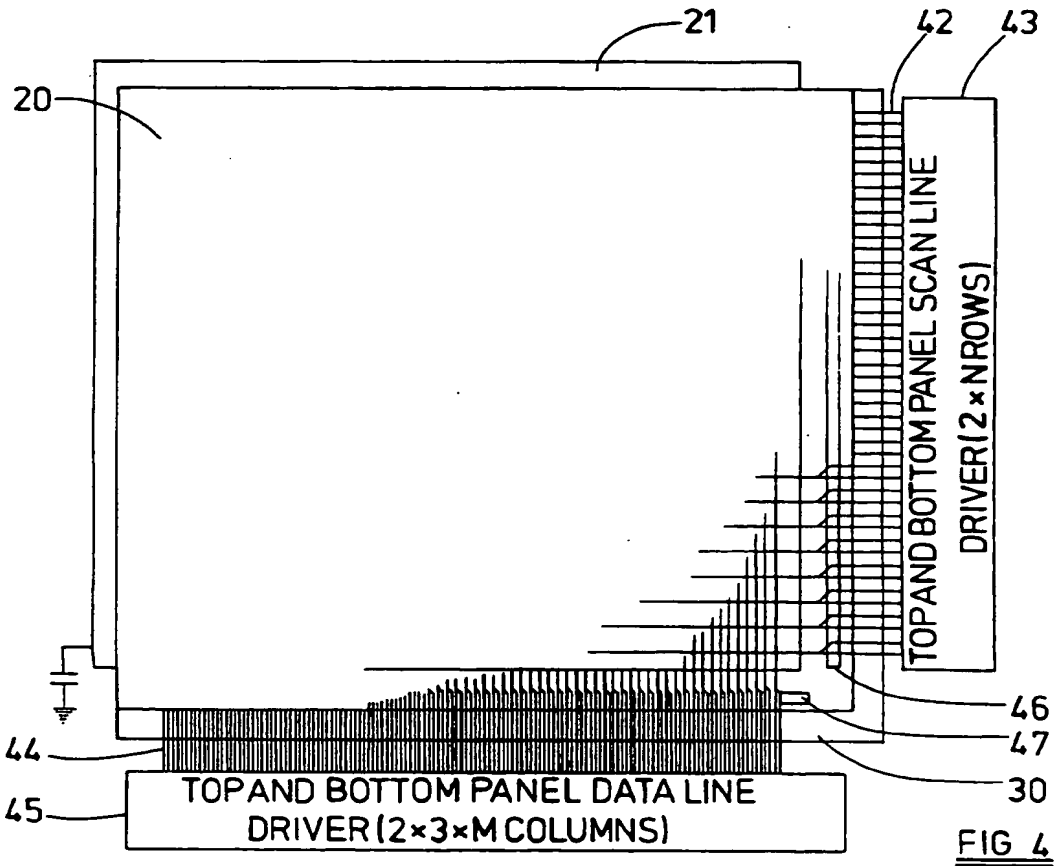
21
42
43
20
TOP AND BOTTOM PANEL SCAN LINE
DRIVER (2×N ROWS)
46
47
44
30
45
TOP AND BOTTOM PANEL DATA LINE
DRIVER (2×3×M COLUMNS)

FIG 4

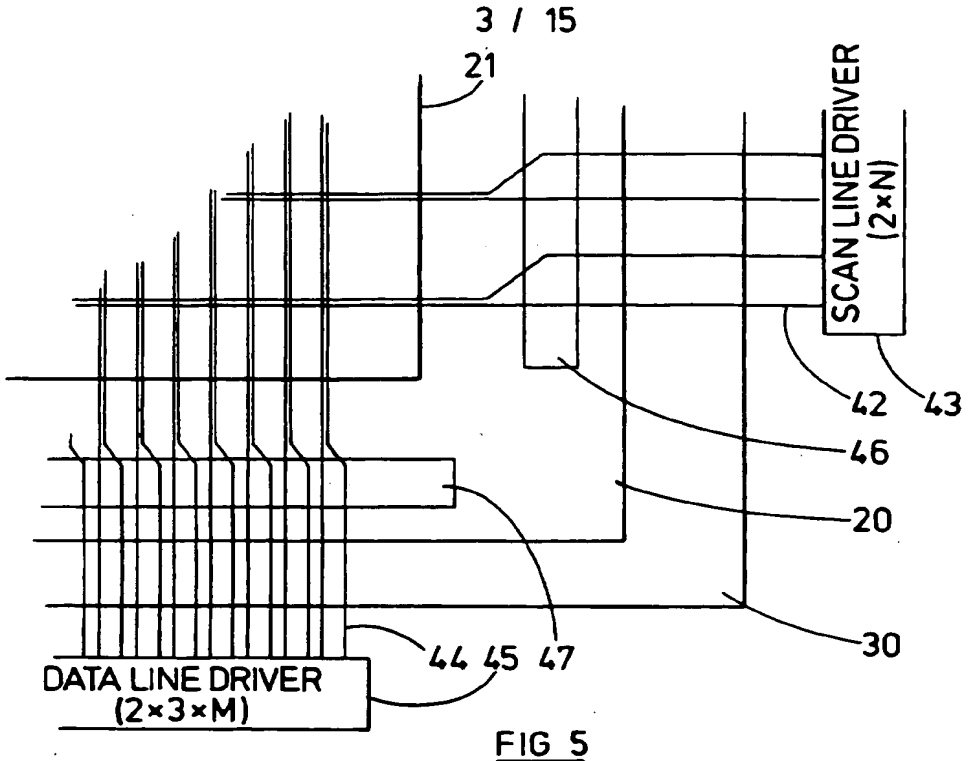

FIG 5

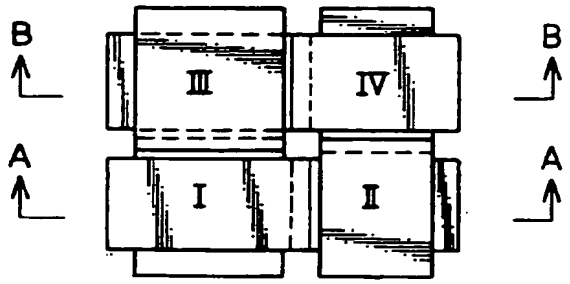

FIG 6a

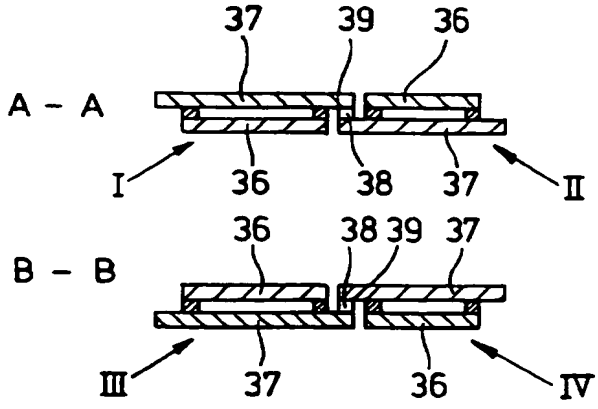

FIG 6b

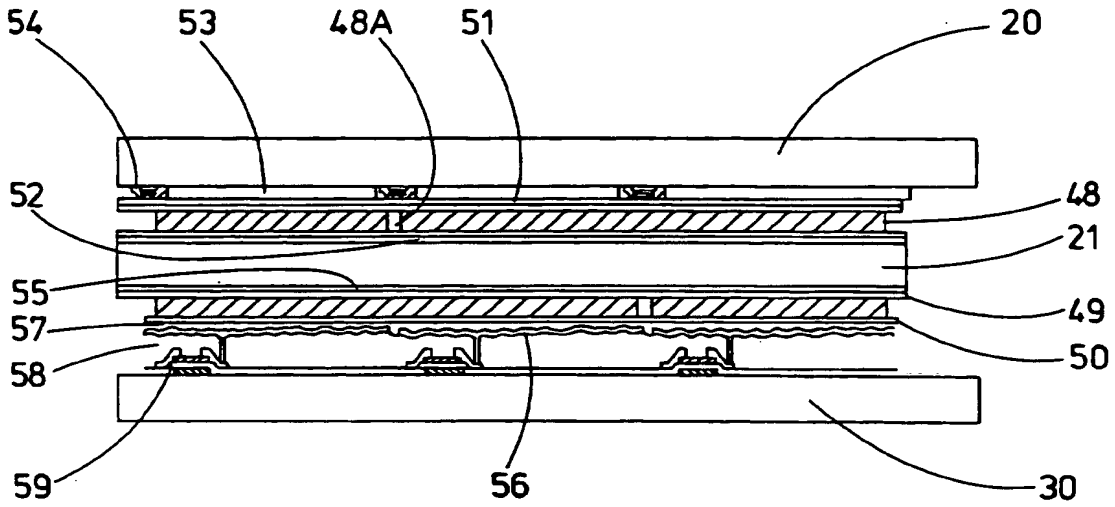
54
53
48A
51
20
52
48
21
55
49
57
50
58
59
56
30

FIG 7

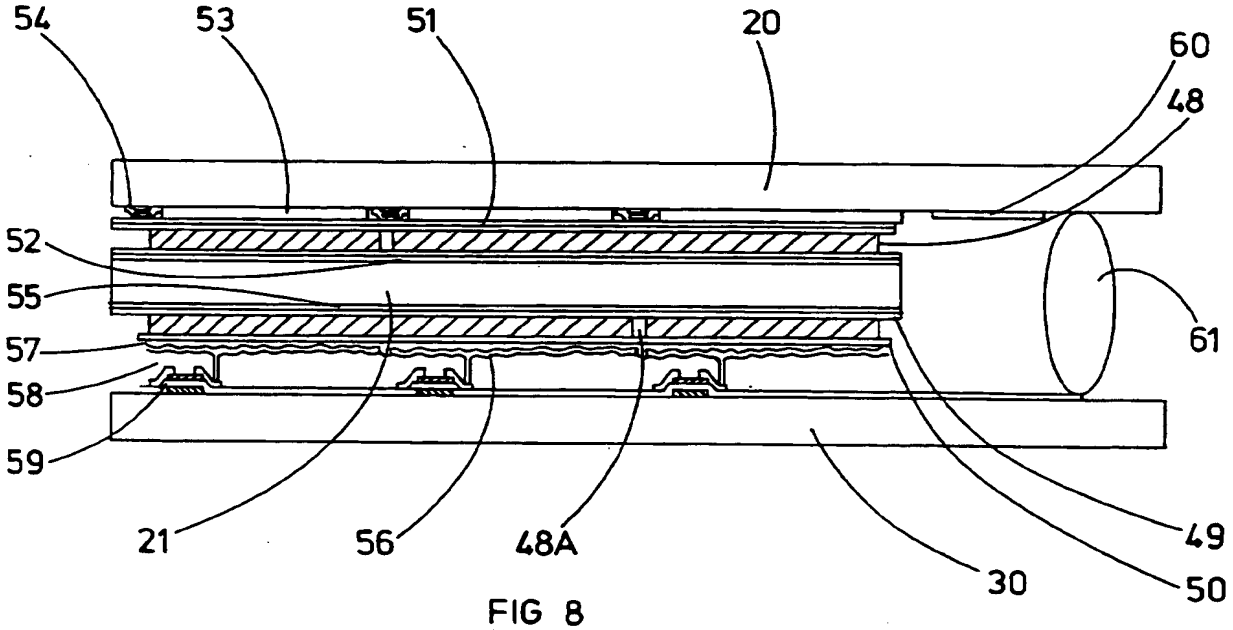
54
53
51
20
60
48
52
55
61
57
58
59
21
56
48A
49
30
50

FIG 8

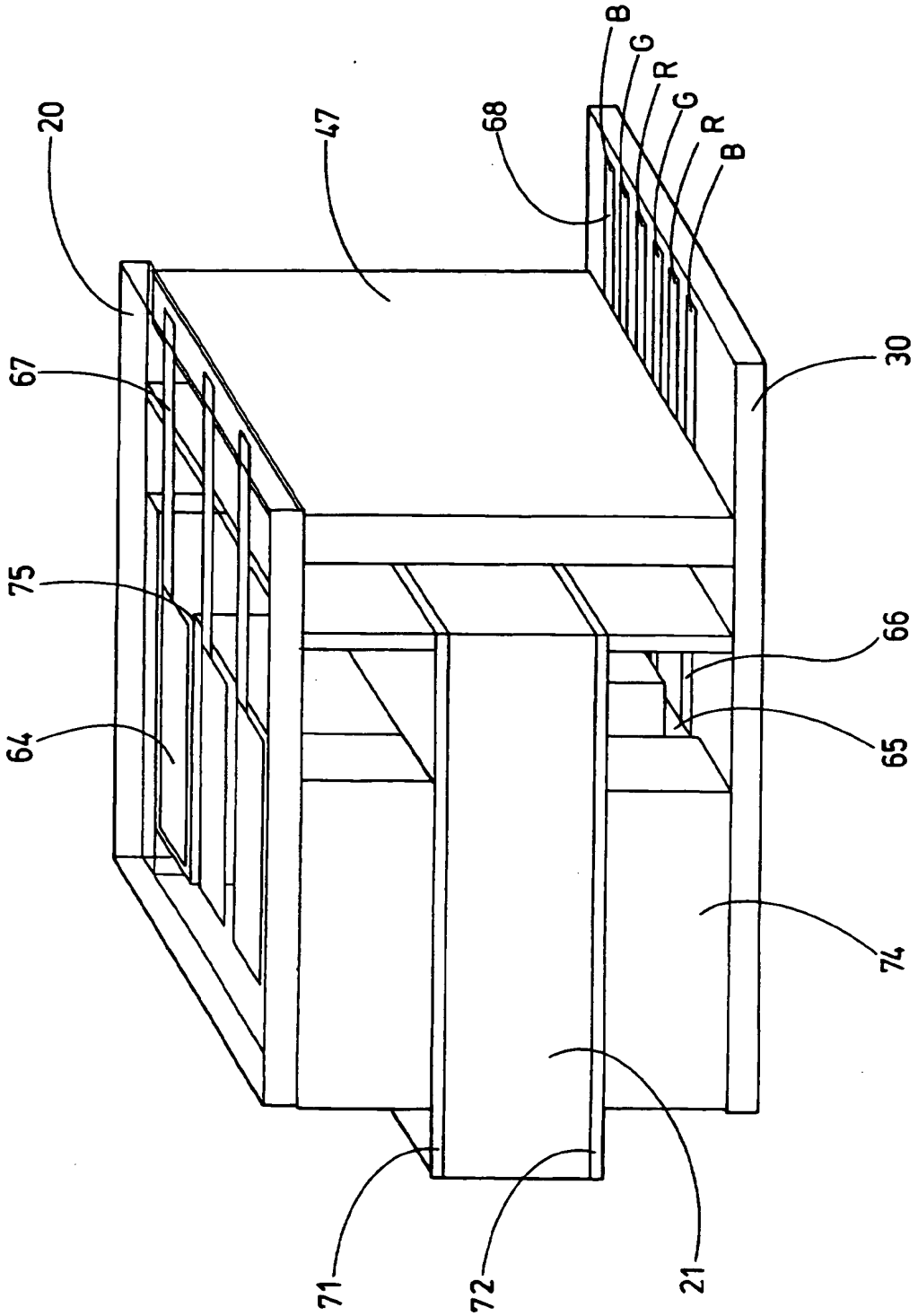

FIG 9

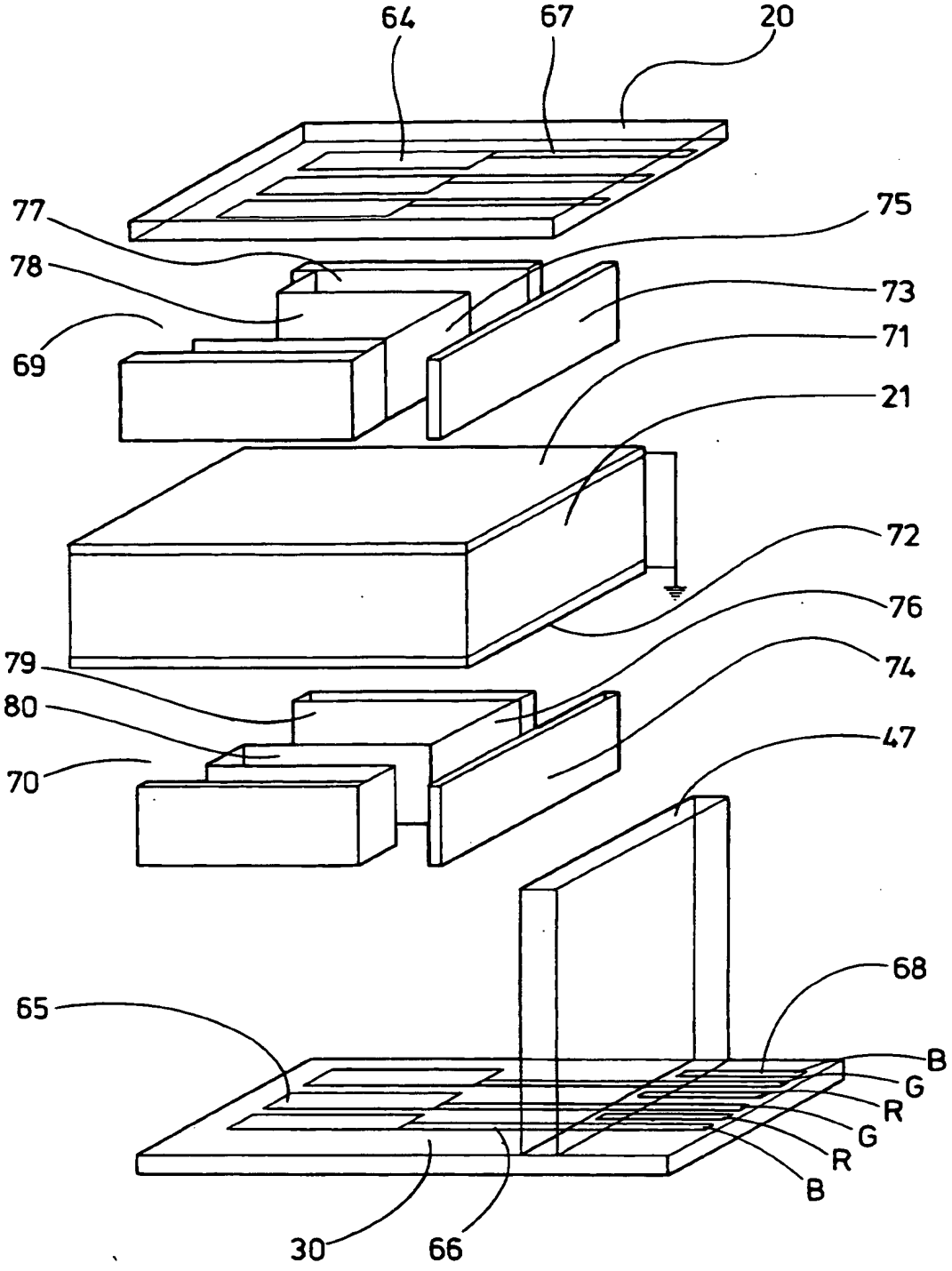

FIG 10

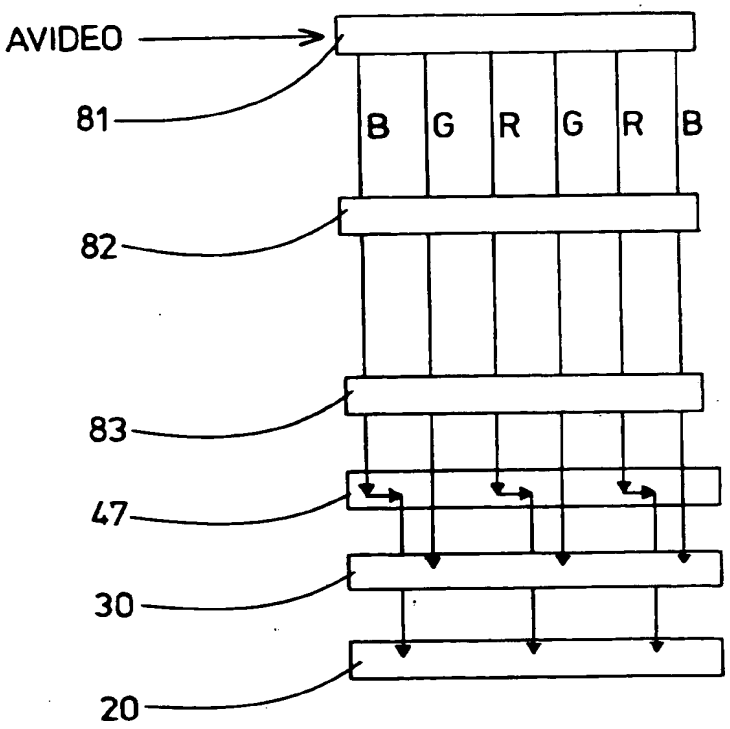
AVIDEO
81
B
G
R
G
R
B
82
83
47
30
20

FIG 11

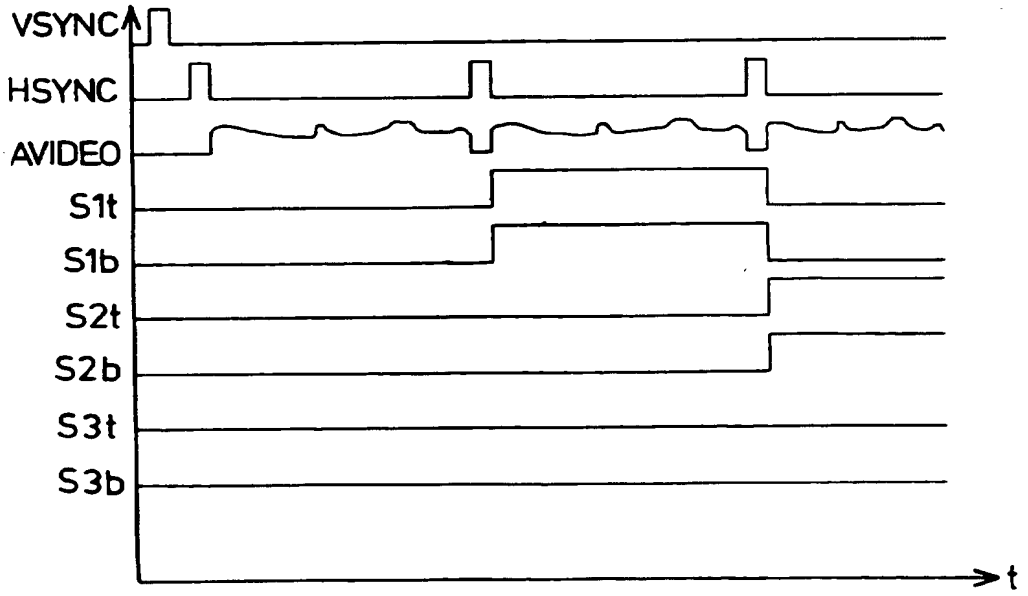
VSYNC
HSYNC
AVIDEO
S1t
S1b
S2t
S2b
S3t
S3b
t

FIG 12

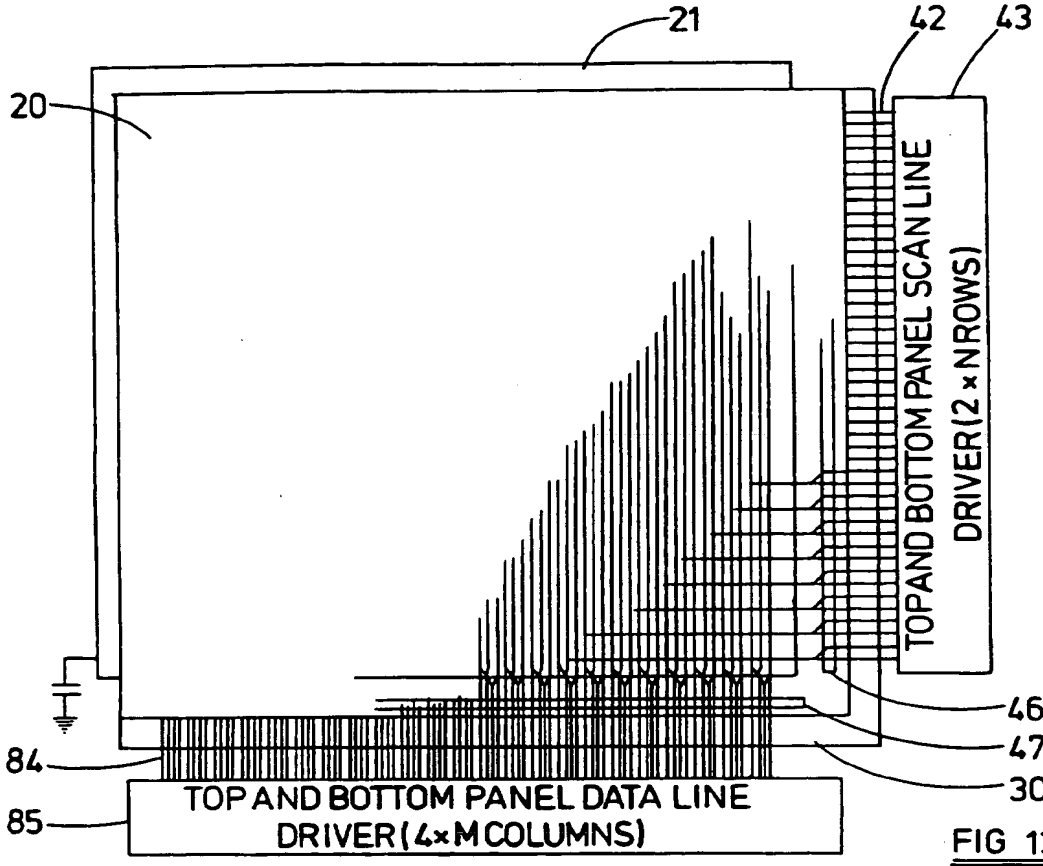
21
42
43
20
TOP AND BOTTOM PANEL SCAN LINE DRIVER (2×N ROWS)
46
47
84
30
85
TOP AND BOTTOM PANEL DATA LINE DRIVER (4×M COLUMNS)

FIG 13

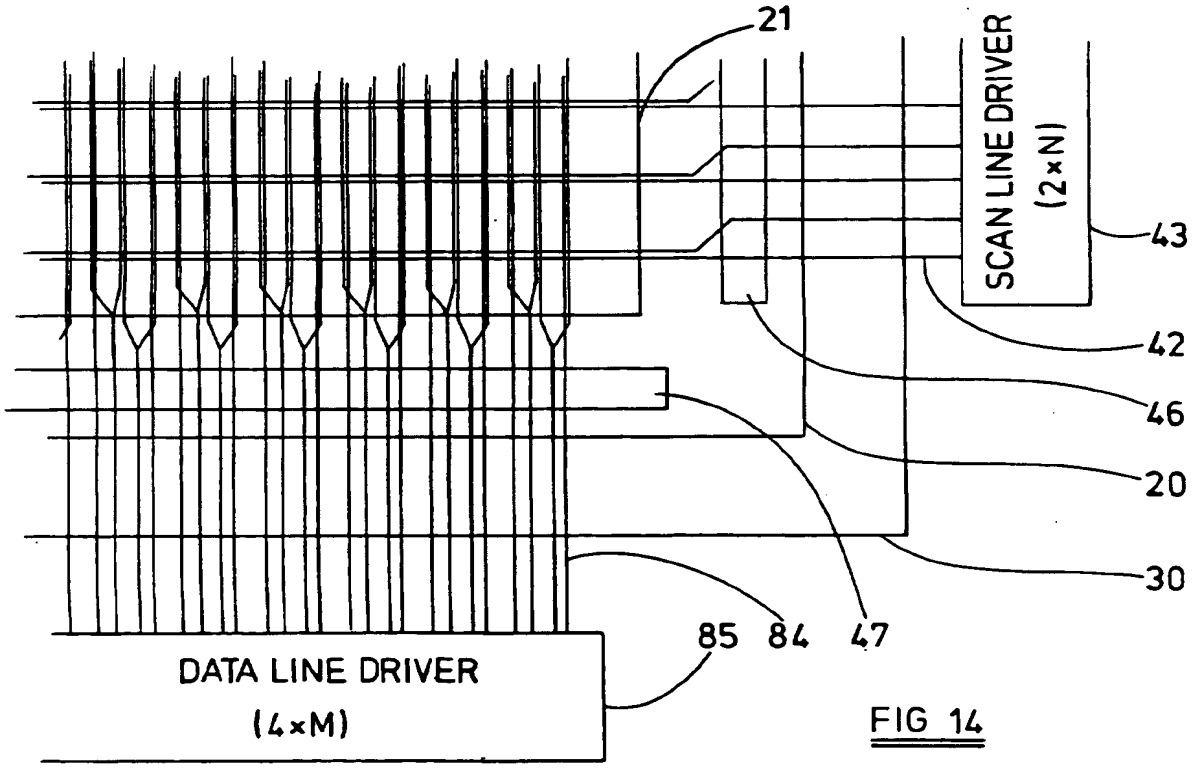
21
SCAN LINE DRIVER (2×N)
43
42
46
20
30
85
84
47
DATA LINE DRIVER (4×M)

FIG 14

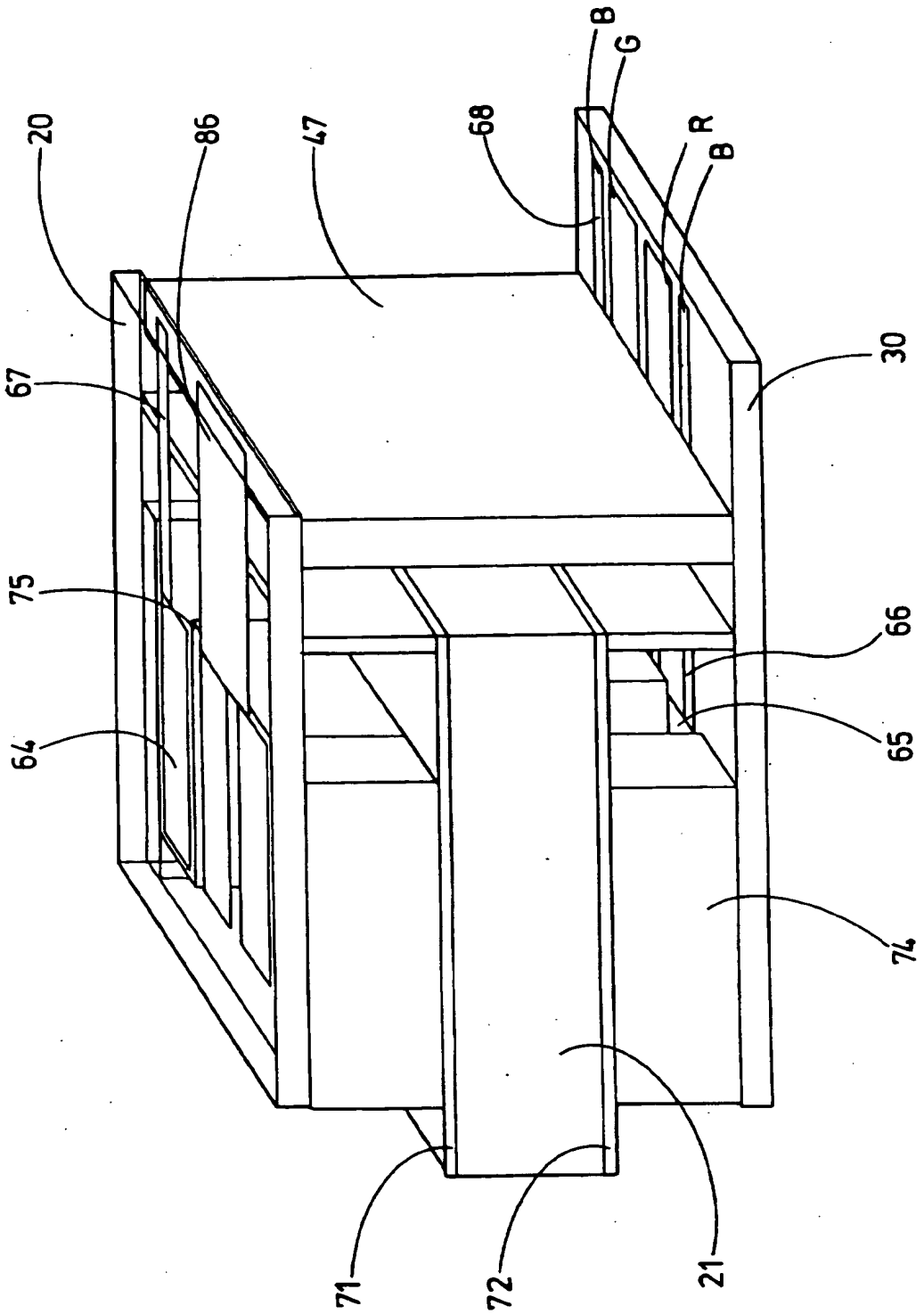

FIG 15

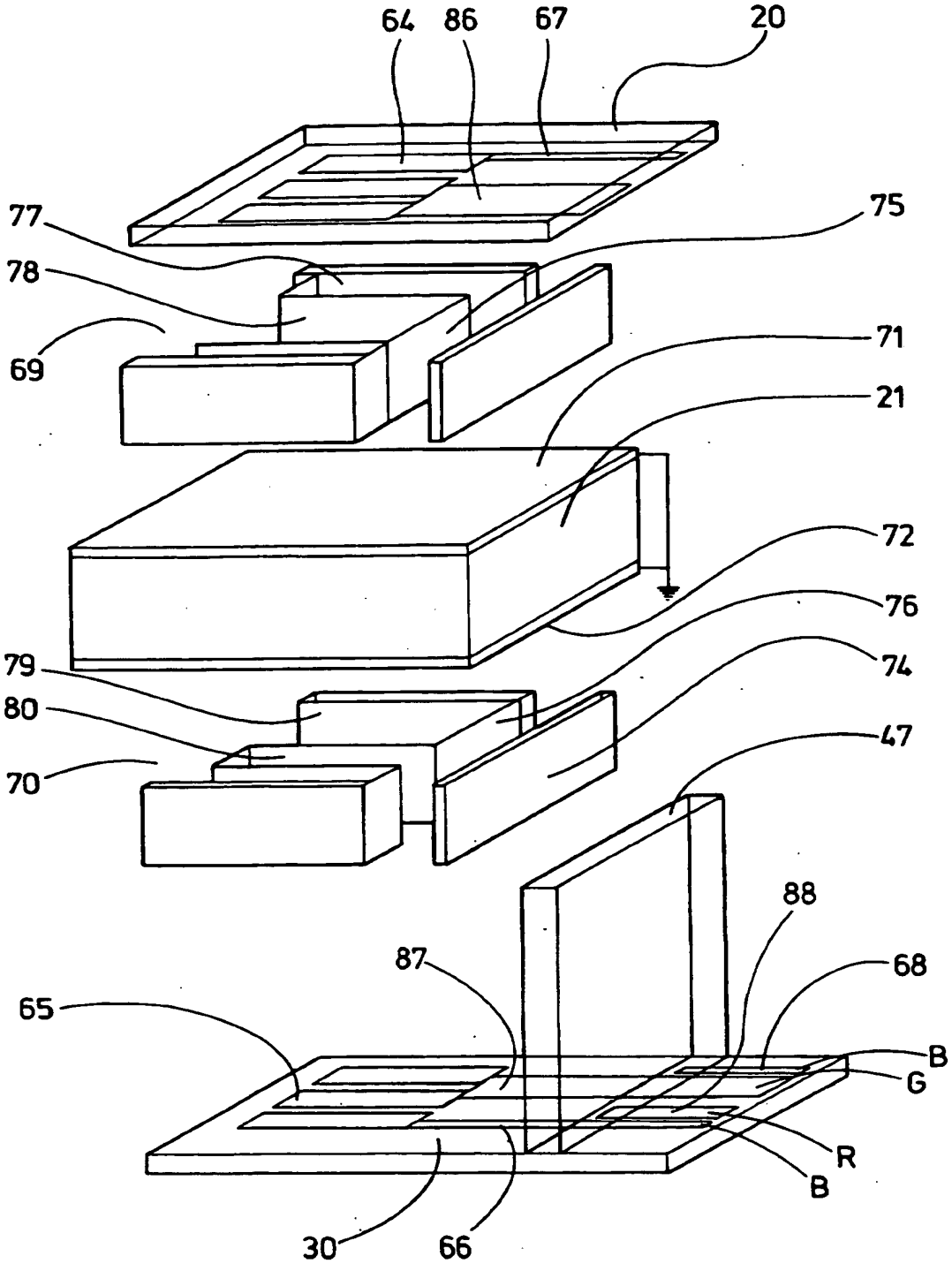
64
86
67
20
77
75
78
69
71
21
72
76
79
74
80
47
70
88
87
68
65
B
G
R
B
30
66

FIG 16

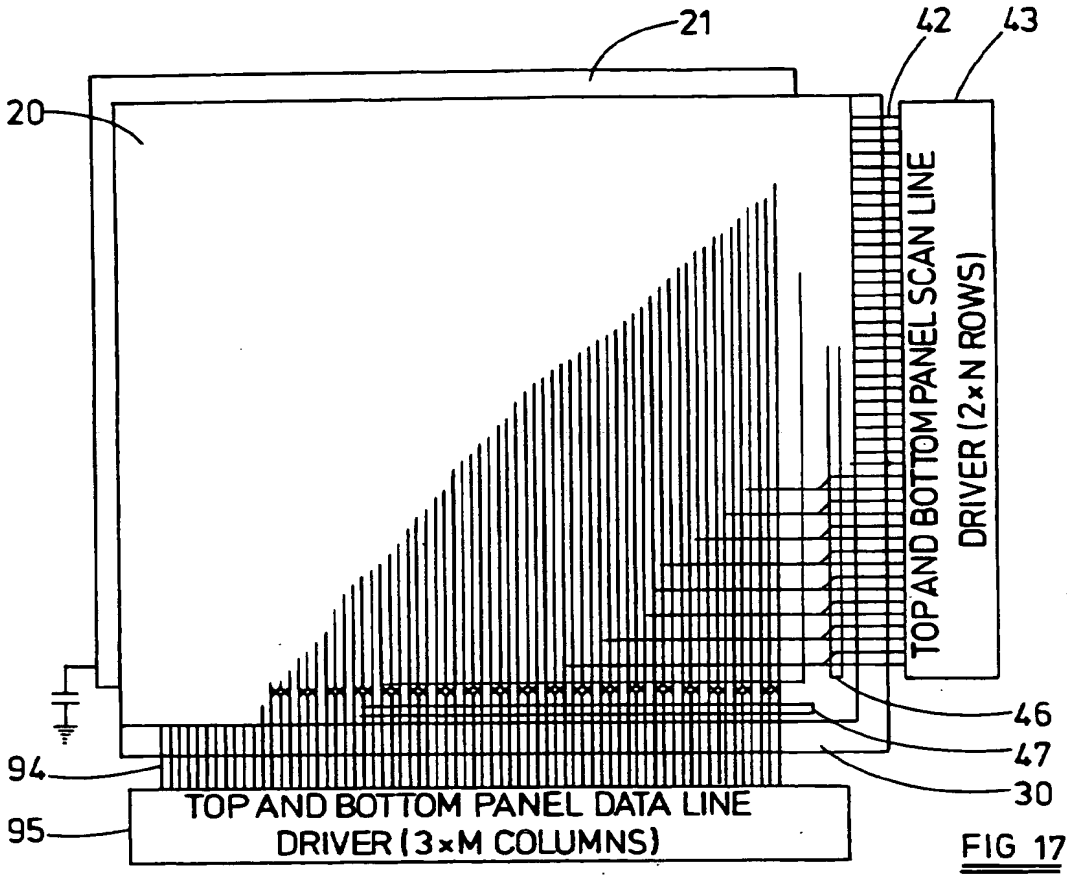
21
42
43
20
TOP AND BOTTOM PANEL SCAN LINE DRIVER (2×N ROWS)
46
47
30
94
95
TOP AND BOTTOM PANEL DATA LINE DRIVER (3×M COLUMNS)

FIG 17

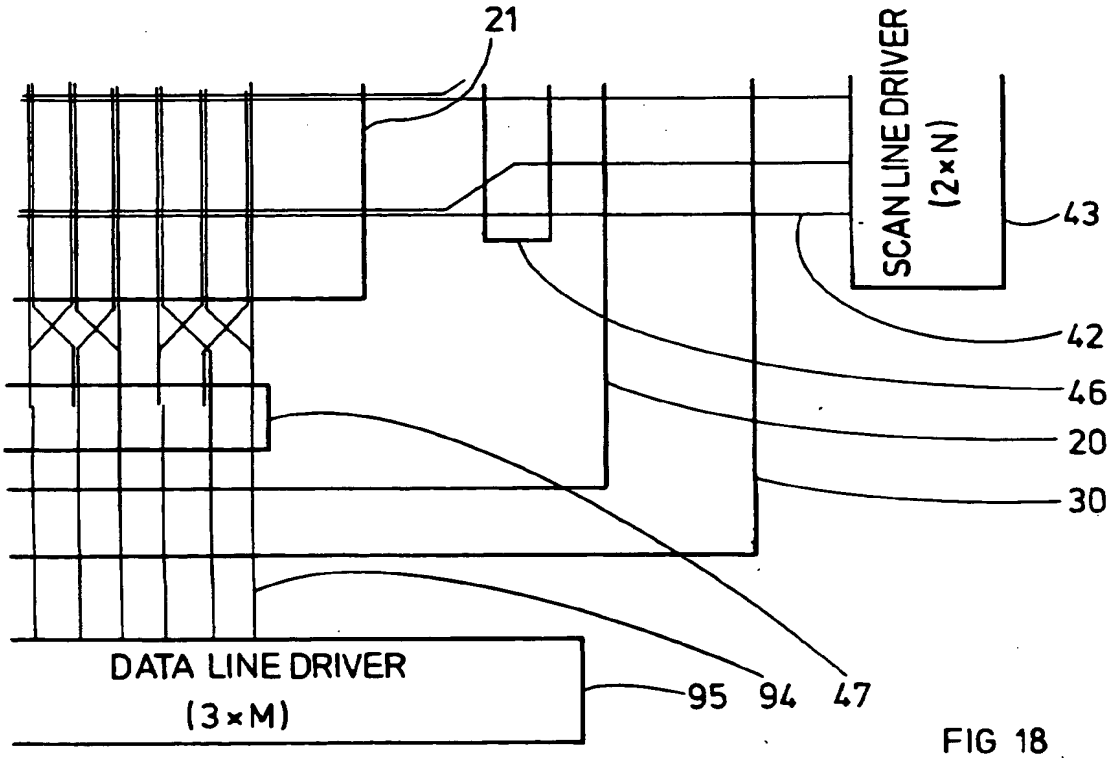
21
SCAN LINE DRIVER (2×N)
43
42
46
20
30
DATA LINE DRIVER (3×M)
95
94
47

FIG 18

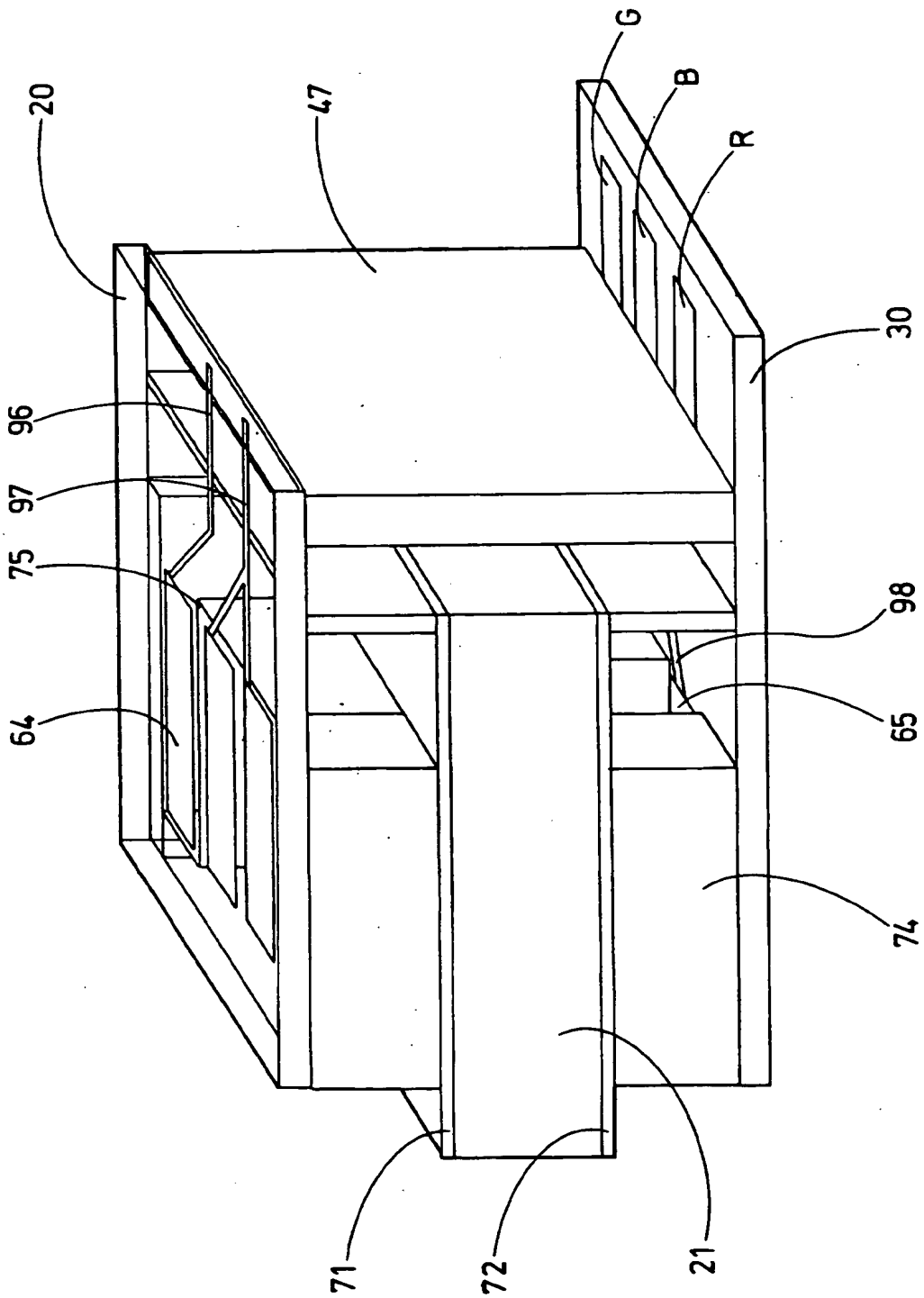

FIG 19

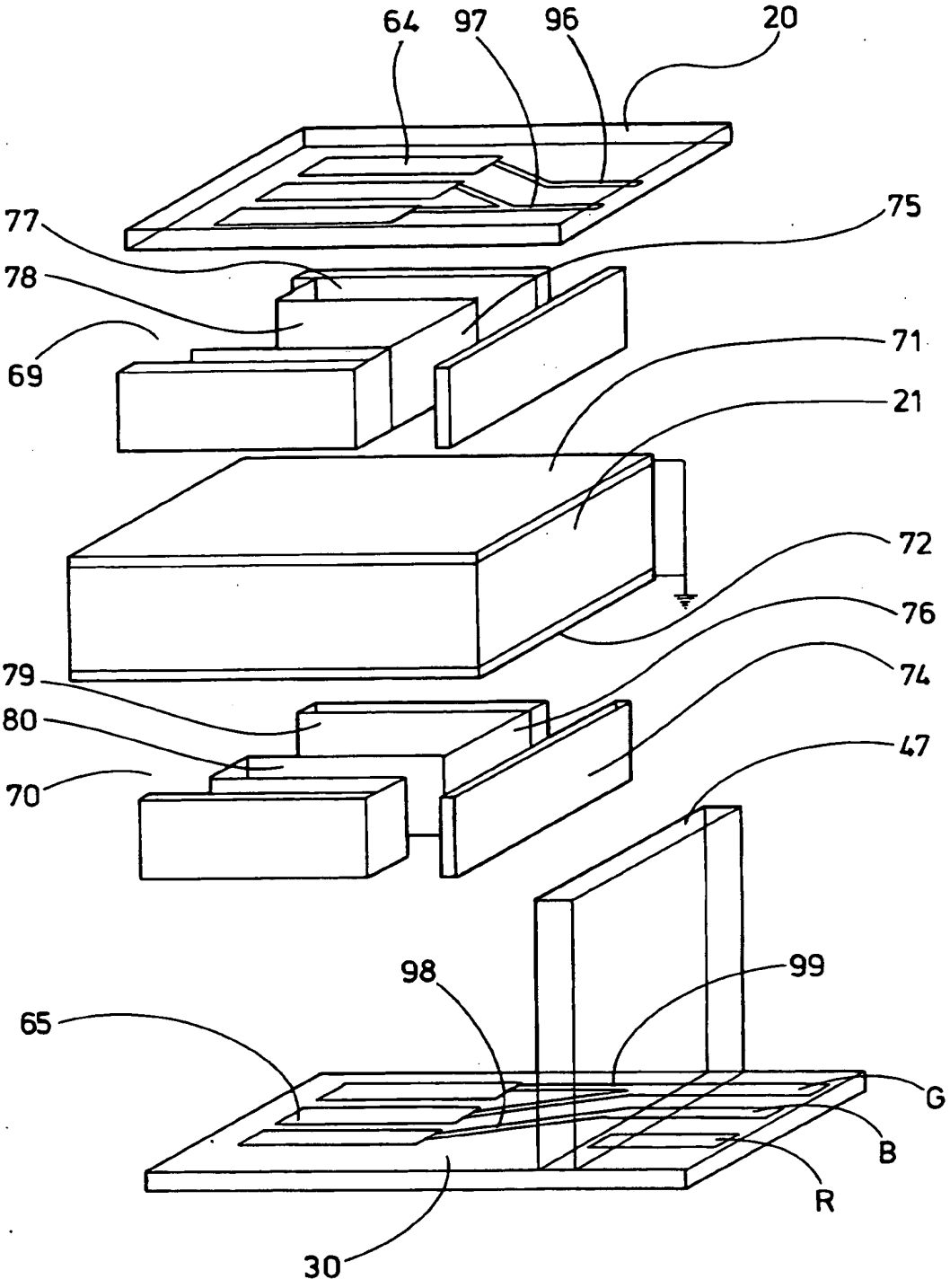

FIG 20

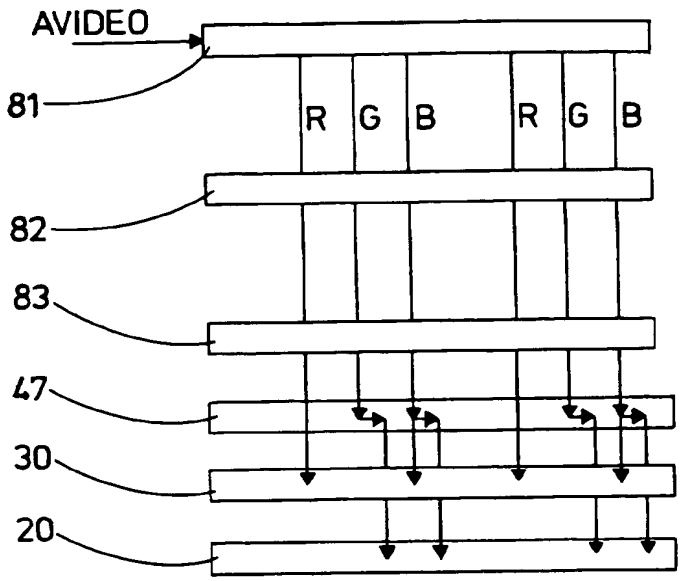
AVIDEO
81
R G B R G B
82
83
47
30
20

FIG 21

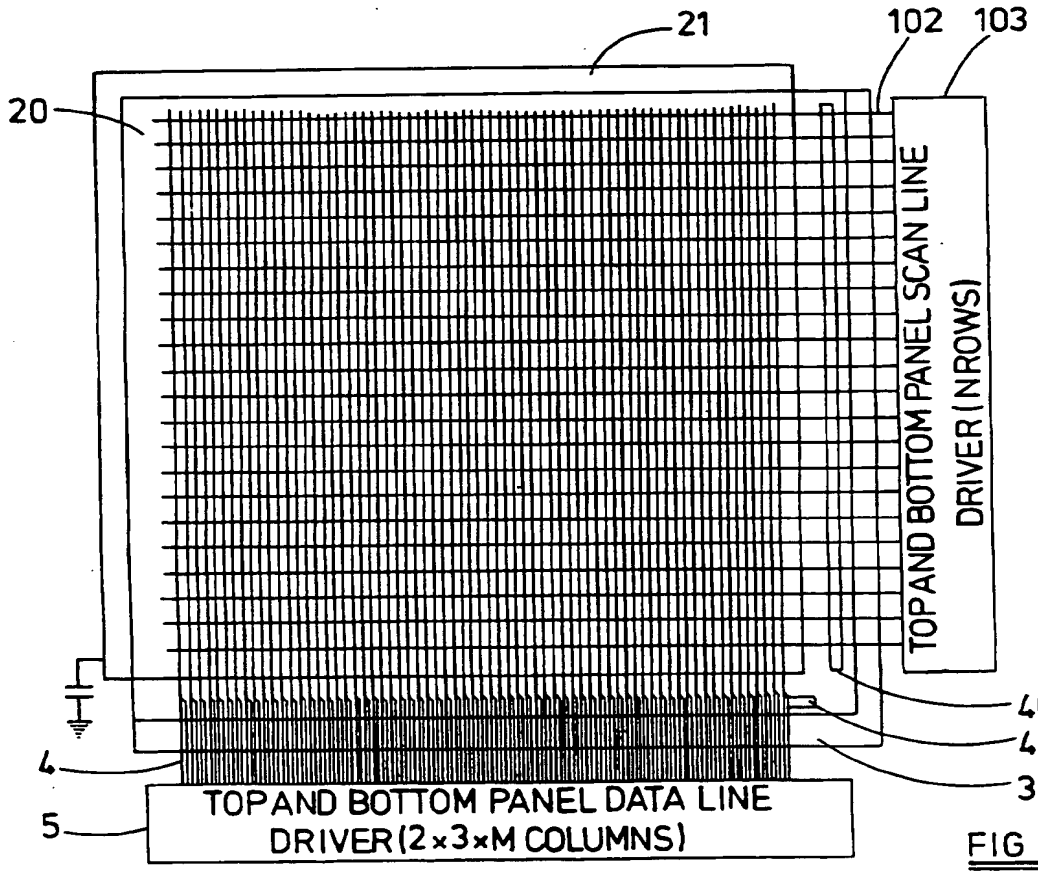
21
102
103
20
TOP AND BOTTOM PANEL SCAN LINE DRIVER (N ROWS)
46
47
30
4
5
TOP AND BOTTOM PANEL DATA LINE DRIVER (2×3×M COLUMNS)

FIG 22

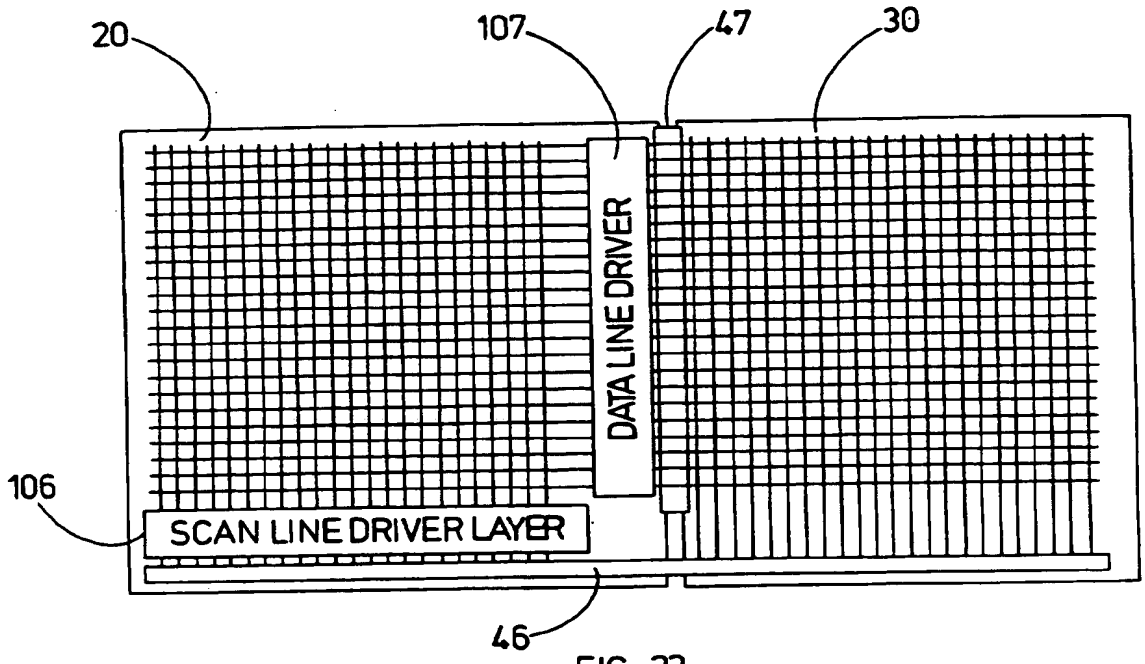
20
107
47
30
DATA LINE DRIVER
106
SCAN LINE DRIVER LAYER
46

FIG 23

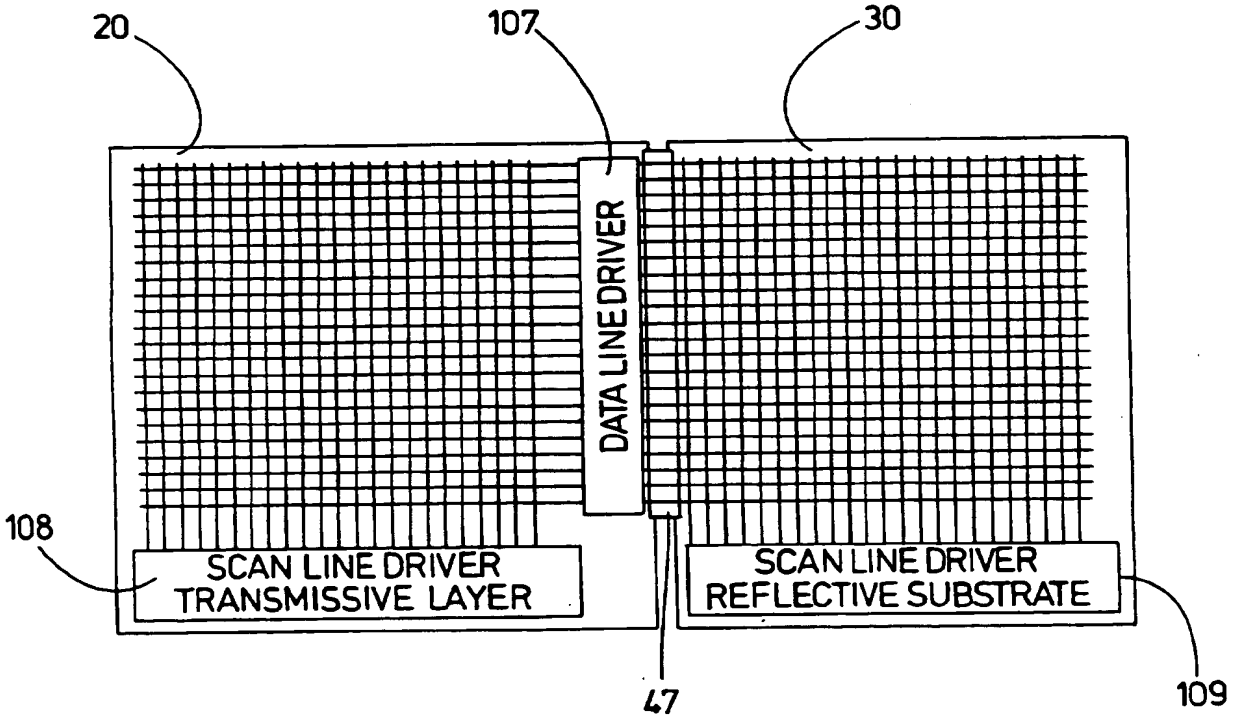
20
107
30
DATA LINE DRIVER
108
SCAN LINE DRIVER
TRANSMISSIVE LAYER
SCAN LINE DRIVER
REFLECTIVE SUBSTRATE
47
109

FIG 24

Multilayer Display Panels

This invention relates to multilayer display panels and is concerned more particularly, but not exclusively, with multilayer liquid crystal display panels.

The invention is particularly applicable to active matrix liquid crystal displays (AMLCD's) which may be implemented utilising polycrystalline silicon thin film transistors (TFT's) and associated driver circuitry integrated on a common substrate. Figure 1 shows a typical black/white AMLCD 1 composed of N rows and M columns of display elements (pixels) addressable by scan lines 2 connected to a scan line driver circuit 3 and data lines connected to a data line driver circuit 5. Data voltages are applied to the data lines 4 by the data line driver circuit 5 and scan voltages are applied to the scan lines 2 by the scan line driver circuit 3 so that such voltages in combination serve to apply resultant voltages to pixel electrodes 6 in order to control the optical transmission states of the pixels along each row as the rows are scanned in a cyclically repeating sequence.

This is achieved as follows for a single row of pixels. The data line driver circuit 5 reads a line of data to be displayed by the row of pixels and applies corresponding data voltages to the data lines 4 so as to charge up each data line 4 to the required data voltage. The scan line 2 corresponding to the row of pixels to be controlled is activated by the application of the scan voltage by the scan line driver circuit 3 so that a TFT 7 associated with each pixel is switched on to transfer charge from the corresponding data line 4 to a pixel storage capacitor 8 associated with the pixel. When the scan voltage is removed the TFT 7 isolates the pixel storage capacitance 8 from the data line 4 so that the optical transmission state of the pixel corresponds to the voltage across the pixel storage capacitance 8 until the pixel is refreshed during the next scanning frame. The rows of pixels are refreshed one at a time until all the rows have been refreshed to complete refreshing of a frame of display data. The process is then repeated for the next frame of data.

British Patent Application No. 9706942.1 (96056SLE) discloses driver circuitry for such AMLCD which utilises only a single data memory for each data line and which can therefore be implemented in a particularly compact and area efficient manner. Such driver circuitry may be based either on a split scan line driving scheme or on a switchable data line bank driving scheme.

The data line driver circuit 5 is controlled by a liquid crystal display (LCD) controller supplying an output voltage related to its input voltage in a manner determined by the electrooptic curve of the particular liquid crystal mode used. The data line driver and scan line driver circuits should be fabricated from a semiconductor material of sufficient mobility, such as crystalline silicon, and can be mounted either on the glass substrate by chip on glass (COG) technology, or on a flexible plastics strip folded behind the display panel and connected to the substrate using tape automated bonding (TAB). The use of TFT's of higher charge carrier mobility fabricated, for example, from polycrystalline silicon or CdSe offers the possibility of fabricating the driver circuitry directly on the glass substrate using the same semiconducting material, as disclosed, for example, in US Patent No. 5250931. For single layer AMLCD's this may be used to reduce bezel size and possibly to provide higher reliability, lower manufacturing cost and higher pixel aperture ratio.

Figure 2 shows a typical transmissive colour AMLCD 10 in which each pixel is divided into three subpixels, each controlling one of the primary colours, red (R), green (G) and blue (B). The AMLCD 10 is in this case composed of N rows and 3 M columns of subpixels addressable by scan lines 12 connected to a scan line driver circuit 13 and data lines 14 connected to a data line driver circuit 15. Furthermore, the optical transmission states of the subpixels, R, G and B are controlled by the application of corresponding data and scan voltages to respective subpixel electrodes 16 by way of associated subpixel TFT's 17 and storage capacitors 18, in a similar manner to that already described above with a reference to Figure 1. As is well known, the control of

the transmission states of the three colour subpixels enables the required colour balance to be obtained in the displayed image.

Furthermore it is known to make use of a double layer colour AMLCD having the general structure shown in Figure 3 in certain cases.

Such a double layer AMLCD comprises a first layer constituted by a top active matrix substrate 20 and a second layer constituted by a bottom active matrix substrate 30 separated by a conducting divider 21. The top active matrix substrate 20 is composed of N rows and 3 M columns of subpixels addressable by scan lines 22 connected to a top scan line driver circuit 23 and data lines 24 connected to a top data line driver circuit 25. Furthermore the bottom active matrix substrate 30 comprises N rows and 3 M columns of subpixels addressable by scan lines 32 connected to a bottom scan line driver circuit 33 and data lines 34 connected to a bottom data line driver circuit 35. Each of the top and bottom active matrix substrates 20, 30 comprises a matrix of subpixel electrodes 26 and associated subpixel TFT's 27 addressable by scan and data voltages supplied by the scan and data lines 22, 24 or 32, 34, as in the single layer arrangement described above with reference to Figure 2. Such a double layer arrangement relies on the subpixels of the two layers being exactly juxtaposed and uses four driver circuits 23, 25, 33, 35 connected to the four sides of the panel. However the use of four such driver circuits not only increases circuit complexity and manufacturing cost, but is also disadvantageous in that it decreases the manufacturing yield and the long term reliability of the panel.

US Patent No. 5015074 discloses use of a double layer colour AMLCD in which colour production is distributed between the subpixels of the two layers in order to produce higher reflectivity, so that two of the primary colours are controlled by subpixels in respective layers, whereas the third primary colour is controlled by subpixels in both layers. Such a display can produce an intrinsic greyscale using half of the pixel area for each colour triad switched.

US Patent No. 5164853 discloses a tiled large screen liquid crystal display consisting of a plurality of liquid crystal panel elements disposed adjacent one another. Figure 6a is a plan view of part of such a liquid crystal display showing four panel elements I, II, III and IV disposed in overlapping relationship relative to one another. A may be seen in Figure 6b showing sections along the lines A-A and B-B in Figure 6a, each panel element comprises two substrates 36, 37 between which the liquid crystal material is contained, the substrates of adjacent panels overlapping one another and being interconnected by a resin layer 39 containing conductive particles 38 so as to form an anisotropic conductor. Scan and data voltages are supplied from one panel element to another by way of the anisotropic conductors located at the overlapping bezel areas of the elements. Since the data and scan voltages applied to adjacent cells are the same, it follows that the cells cannot be controlled independently of one another.

US Patent No. 4556286 discloses a multilayer guest-host liquid crystal display comprising two or more layers separated by conducting or non-conducting dividers. However no details of fabrication of such an arrangement are disclosed.

US Patent No. 5250931 discloses a single layer AMLCD in which polycrystalline silicon Tuft's and associated driver circuits are integrated on a single substrate. Such an arrangement is intended to overcome the problem of reduced aperture ratio in high density projection displays by reducing the TFT size, and to reduce the panel size by integration of the driver circuits so as to remove the need for high density connectors at the edges of the panel. The intention is also to reduce manufacturing costs by reducing the number of interconnections to be made, and to overcome the problem of low reliability due to the increased probability of failure when a large number of interconnections are used.

It is an object of the invention to provide a multilayer display panel in which the number of interconnections between the panel and associated driver circuitry is decreased.

The invention is defined by the accompanying claims.

By providing common driver circuit means for addressing the first and second layers by means of the first and second connecting terminals supplying data and/or scan signals to respective edge regions of the layers, it is possible to ensure that the number of interconnections from the scan line and data line driver circuitry to the panel is decreased as compared with a conventional multilayer display panel arrangement, such as that described with reference to Figure 3 above in which four driver circuits are provided along the fours sides of the panel. By contrast, in a preferred arrangement of the invention, it is possible to provide a scan line driver circuit along one side of the panel having common scan line connecting terminals, and/or a data line driver circuit along another side of the panel having common data line connecting terminals. In such an embodiment data voltages may be supplied to the data lines of the second matrix connected directly to second connecting terminals of the data line driver circuit and scan voltages may be supplied to the scan lines of the second matrix connected directly to the second connecting terminals of the scan line driver circuit, whereas data and scan voltages may be supplied to the data and scan lines of the first matrix from the first connecting terminals of the two driver circuits by way of respective conducting elements, such as anisotropic conductors constituted by z-conducting adhesive tape or glue, for example.

In order that the invention may be more fully understood, reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 is a schematic representation of a single layer black/white AMLCD in accordance with the prior art;

Figure 2 is a schematic representation of a single layer colour AMLCD in accordance with the prior art;

Figure 3 is a schematic representation of a double layer colour AMLCD in accordance with the prior art;

Figure 4 is a schematic representation of a double layer colour AMLCD in accordance with the present invention;

Figure 5 shows an enlarged detail of the double layer colour AMLCD shown in Figure 4;

Figure 6a is a diagrammatic representation of an interconnection arrangement used in a prior art display panel disclosed in US Patent No. 5164853;

Figure 6b is a sectional view of the arrangement of Figure 6a;

Figure 7 is a section through a single pixel of a prior art double layer reflective colour GH-AMLCD as disclosed in US Patent No. 5015074;

Figure 8 is a section through a single pixel of a double layer reflective colour GH-AMLCD in accordance with the invention;

Figure 9 is a schematic view of a single pixel of the GH-AMLCD of Figures 4 and 5;

Figure 10 is an exploded view showing the pixel of the GH-AMLCD of Figures 4 and 5 before filling and sealing;

Figure 11 is a schematic representation of the data driver architecture for the double layer GH-AMLCD of Figures 9 and 10;

Figure 12 is a timing diagram for driving a double layer AMLCD using an analogue video input;

Figure 13 is a schematic representation of a further double layer colour GH-AMLCD in accordance with the invention;

Figure 14 is an enlarged detail of the double layer colour GH-AMLCD of Figure 13;

Figure 15 is a schematic view of a single pixel of the GH-AMLCD of Figures 13 and 14;

Figure 16 is an exploded view of the single pixel of Figure 15 prior to filling and sealing;

Figure 17 is a schematic representation of a still further double layer colour GH-AMLCD in accordance with the invention;

Figure 18 is an enlarged detail of the double layer colour GH-AMLCD of Figure 17;

Figure 19 is a schematic view of a single pixel of the GH-AMLCD of Figures 17 and 18;

Figure 20 is an exploded view of the single pixel of Figure 19 prior to filling and sealing;

Figure 21 is a schematic representation of the data driver architecture for the GH-AMLCD of Figures 17-20;

Figure 22 is a schematic representation of a still further double layer colour GH-AMLCD in accordance with the invention;

Figure 23 is a schematic representation of the polycrystalline silicon driver architecture of a AMLCD in accordance with the invention; and

Figure 24 is a schematic representation of the polycrystalline silicon driver architecture of a further AMLCD in accordance with the invention.

Examples of multilayer display panels in accordance with the invention will now be described in which each panel is in the form of a double layer colour GH-AMLCD (guest-host active matrix liquid crystal display) having top and bottom active matrix substrates and using the same LCD controller architecture to adjust the RGB video input signals to the required grey levels independently of the LC mode. However it should be understood that the invention is also applicable to other types of multilayer display panel, particularly to other types of liquid crystal display panel, whether these are of reflective, transmissive or transflective type and whether they are of active matrix or passive matrix type. Furthermore various driver architectures may be used for such display panels, including any of the driver architectures disclosed in British Patent Application No. 9706942.1 (96056SLE), as well as various permutations of location and number of the substrates. In particular the panel may comprise more than two substrates, and the substrates may be located relative to one another such that they are not completely superimposed on one another.

The double layer colour GH-AMLCD in accordance with the invention shown in Figure 4 comprises a top active matrix substrate 20, a bottom active matrix substrate 30 and a conducting divider 21 interposed between the top and bottom substrates 20, 30. By contrast with the prior art arrangement shown in Figure 3, a common scan line driver circuit 43 is provided for applying scan voltages to the top and bottom substrates 20, 30 by way of scan lines 42, and a common data line driver circuit 45 is provided for applying data voltages to the top and bottom substrates 20, 30 by way of data lines 44. The 2 N scan lines 42 and the 2 x 3 M data lines 44 are connected to anisotropic conductors 46 and 47 mounted on the bottom substrate 20 and extending along two mutually perpendicularly extending edges of the substrate 30. The N scan lines of the top substrate 20 are connected by the conductor 46 to the N scan lines of the bottom substrate 30, and the 3 M data lines of the top substrate 20 are connected by the conductor 47 to the 3 M data lines of the bottom substrate 30, as will be described in more detail below with reference to the enlarged detail of Figure 5. It should be noted that the top and bottom substrates 20, 30 and the divider 21 are shown slightly offset in Figures 4 and 5 simply so as to render the figures easier to read, it being understood that the substrates 20, 30 and the divider 21 would in practice be directly superimposed on one another with the pixels of the two layers in register in this embodiment.

Referring to the enlarged detail of Figure 5 each of the anisotropic conductors 46 and 47 is electrically conductive in only one direction, that is in the z-direction which is the direction normal to the two, parallel substrates 20, 30 and hence perpendicular to the length of the conductor 46 or 47, and consists of a band of a z-conducting adhesive located at the bezel area of the panel by means of which the scan lines or data lines, as the case may be, of the top substrate 20 are connected to the corresponding scan lines 42 or data lines 44. However it will be appreciated that the pitch of the connecting lines of the scan line and data line driver circuits 43, 45 in this embodiment is decreased as compared with the case where driver circuits are provided on all four sides of the panel. A possible material for the conductors 46 and 47 is 50 μm thick adhesive tape of the type supplied by 3 M as "Scotch 9703 Conductive Adhesive Transfer Tape" having an ac impedance of 0.44 Ohms and an insulation resistance of more than 10^{14} Ohms.

Alternatively an epoxy-based adhesive loaded with gold coated polystyrene spheres of the type supplied by Elatech, Germany may be used.

Figure 7 shows a section through a single pixel of a known two layer reflective GH-AMLCD, as disclosed, for example, in US Patent No. 5015074, with the column (data) electrodes being shown correctly but the row (scan) electrodes being simplified (rather than being shown in the correct manner as extending transversely to the column electrodes) in order to render the figure easier to read. The AMLCD comprises a top, transmissive substrate 20 and a bottom, reflective substrate 30, as well as a divider 21 interposed therebetween. The pixel comprises two subpixels on each substrate 20, 30, each subpixel consisting of liquid crystal material 48 bounded by separating walls 48A and alignment layers 49 and 50, and two of the primary colours are controlled by respective (large) subpixels in respective layers, whereas the third primary colour is controlled by (small) subpixels in both layers. Furthermore transparent electrodes 51 and 52 are provided on both sides of the subpixels of the upper layer, with the electrode 51 being bonded to layer 53 containing the associated TFT's 54. Furthermore a transparent electrode 55 and a reflecting electrode 56 are provided on opposite sides of the subpixels of the lower layer, with a planarisation layer 57 being provided adjacent the reflecting electrode 56, and a roughened polymer layer 58 containing buried TFT's 59 being provided between the reflecting electrode 56 and the substrate 30.

Figure 8 is a section through a single pixel of a two layer reflective GH-AMLCD in accordance with the invention in which like parts are denoted by the same reference numerals as in Figure 7. In this case the transmissive substrate 20 is a glass substrate and the TFT's 54 are fabricated from polycrystalline silicon. Furthermore the scan line driver circuit 60 is integrated with the substrate 20 and the scan lines of the lower substrate 30 are supplied with scan voltages from the scan line driver circuit 60 by way of z-conducting adhesive 61. The data line driver circuit and associated connectors are not shown in the figure.

Figures 9 and 10 show a single pixel of a practical implementation of the embodiment of Figures 4 and 5 comprising three subpixel electrodes 64 on the top substrate 20 and three subpixel electrodes 65 on the bottom substrate 30, the subpixel electrodes 65 being supplied with data voltages by data lines 66 and the subpixel electrodes 64 being supplied with data voltages by data lines 67 connected by the anisotropic conductor 47 to connecting lines 68 disposed intermediate the data lines 66 at the edge of the bottom substrate 30. The top and bottom substrates 20, 30 are separated by two layers 69 and 70 of liquid crystal material disposed on opposite sides of a divider 21 provided with top and bottom conductive coatings 71 and 72. Each liquid crystal layer 69, 70 is bounded at its edges by sealing walls 73 and 74 and is subdivided by folded separating walls 75 and 76. The wall 75 divides the liquid crystal layer 69 into a region 77 corresponding to one (small) subpixel and region 78 corresponding to the other large subpixel of the top substrate 20, and the wall 76 divides the liquid crystal layer 70 into a region 79 corresponding to one (large) subpixel and region 80 corresponding to the other (small) subpixel of the bottom substrate 30. Although not specifically shown in Figures 9 and 10, a monolithic data line driver circuit is fabricated on a high mobility semiconductor substrate edge-connected to the bottom substrate 30 so as to supply the data voltages to the data lines 66 on the bottom substrate 30, as well as to the data lines 67 on the top substrate 20 by way of the connecting lines 68 and the anisotropic conductor 47. A similar arrangement may be provided for supply of the scan voltages to the top and bottom substrates 20, 30.

In one embodiment the GH-AMLCD works in a normally black (NB) mode and an AMLCD controller, comprising a look-up table, adjusts the RGB video input to the required grey level for each subpixel according to the RGB colour co-ordinate. The NB mode requires the data voltage for a primary colour to be applied to two juxtaposed subpixels exhibiting absorption of this primary colour. In an alternative embodiment the AMLCD works in a normally white (NW) mode. The NW mode requires exhibiting substantially no absorption of colour if no voltage is applied.

Figure 11 indicates diagrammatically the application of two sets of RGB signals to capacitative storage elements 81 and 82 and line buffers 83, and the application of the output signals to the top and bottom substrates 20, 30, such that one blue (B) signal and two red (R) signals are applied to the top substrate 20 and two green (G) signals and one blue signal are applied to the bottom substrate 30. In the case of the embodiment working in the NW mode, for example, the R signal is applied to the centre subpixel and the right subpixel of the top substrate 20 in order to modify the red reflectivity, as well as to the top and bottom left subpixel for saturation, as shown in Figure 11. By contrast, in the case of the NB mode embodiment, the R signal is applied to the centre subpixel and the right subpixel of the bottom substrate 30 in order to modify the red reflectivity. In both embodiments the red, green and blue subpixels of the pixel as a whole are individually controlled by the appropriate data voltages.

Figure 12 is a timing diagram showing the data voltages S1t, S2t and S3t applied to the three subpixel electrodes 64 of the top substrate 20 and the data voltages S1b, S2b and S3b applied to the three subpixel electrodes 65 of the bottom substrate 30 in response to an analogue video input AVIDEO and synchronisation signals VSYNC and HSYNC applied to appropriate driver circuitry for driving the two layers simultaneously. The same controller can be used to handle the RGB video input whether the liquid crystal material operates in the normally white (NW) or normally black (NB) mode. These embodiments allow a decrease in the complexity of the controller as the controller is required to adjust for grey level only.

Figure 13 is a schematic diagram, similar to that of Figure 4, of a further embodiment of the invention, Figure 14 showing an enlarged detail of this embodiment. In this case a common data line driver circuit 85 is connected to the top and bottom substrates 20, 30 by 4 M data lines 84, which provides a reduction of 33% in the number of connecting lines as compared with the embodiment of Figures 4 and 5. Such a reduction in the number of connecting lines to the panel is advantageous as it increases the pitch of the connecting lines, and thereby tends to simplify manufacture and increase manufacturing yield. This is achieved by applying the same data voltage to two of the

three subpixel electrodes in each layer which is possible since two subpixel electrodes in each layer are used for controlling the same primary colour. For example, referring to Figure 11, it will be seen that the centre and right subpixels of the top substrate 20 receive the same signal R, and the left and centre subpixels of the bottom substrate 30 receive the same signal G so that the signal R or signal G, as the case may be, may be supplied to the appropriate subpixels by a single data line.

Figures 15 and 16 show a single pixel of a practical implementation of this embodiment, like reference numerals being used to denote the same parts in Figures 9 and 10. In this case it will be seen that a single common data line 86 is used to supply the signal R to two adjacent subpixel electrodes 64 of the top substrate 20, and a common data line 87 is used to supply the signal G to two adjacent subpixel electrodes 65 of the bottom substrate 30. Furthermore a common connecting line 88 on the bottom substrate 30 is used to supply the signal R to the data line 86 on the top substrate 20 by way of the anisotropic conductor 47. The associated AMLCD controller, comprising a look-up table, adjusts the RGB video input to the required grey level for each pair of subpixels according to the RGB colour co-ordinate, thereby reducing the number of data connecting lines by 33% as mentioned above.

The data voltages for the subpixels are generated independently of one another by a separate driver chip which is TAB bonded to the panel. It will be appreciated that the pitch of the TAB bonding is increased as compared with the previously described embodiments as the same data voltages are applied to the two red subpixel electrodes of the pixel, just as the same data voltages are applied to the two green subpixels of the pixel, and the same data voltages are applied to the two blue subpixels of the pixel. The TFT's and alignment layers are omitted in Figures 15 and 16.

In one embodiment the AMLCD in accordance with Figures 13 to 16 works in a normally black (NB) mode, and the data voltage for a primary colour to be applied to two juxtaposed subpixels exhibits absorption of this primary colour. For example, the data voltage is applied to the centre and right subpixels on the bottom substrate 30 in

order to modify the red reflectivity. In an alternative embodiment working in a normally white (NW) mode, the panel is driven using a different look-up table to modify the data output voltage according to the required grey level for each pair of subpixel electrodes. For example, the data voltage is applied to the centre and right subpixels on the bottom substrate 30 in order to modify the red reflectivity.

The above described embodiments utilise the anisotropic conductor 47, in the form of a z-conductor (that is a conductor which conducts signals only in the z direction normal to its length), for supplying data signals to the top substrate 20, thereby avoiding the need for an additional data line driver circuit for the subpixels controlling the reflected colour in both layers. However this technique sacrifices some of the accessible colour space.

Figure 17 schematically shows a further embodiment in accordance with the invention, like reference numerals being used to denote the same parts as in Figure 4, and Figure 18 showing an enlarged detail of the figure. In this embodiment a common scan line driver circuit 43 is connected to the panel by 2 N scan lines 42, and a common data line driver circuit 95 is connected to the panel by 3 M data lines. Figures 19 and 20 show a single pixel of a practical implementation of this embodiment, and in particular show a data line 96 and a branched data line 97 on the top substrate 20, and a data line 98 and a branched data line 99 on the bottom substrate 30, for the purpose of supplying the signal R to two of the subpixel electrodes 64 on the top electrode 20 by way of the conductor 47 and the branched data line 97, the signal B to one of the subpixel electrodes 65 on the bottom substrate 30 by way of the data line 98 and one of the subpixel electrodes 64 on the top substrate 20 by way of the conductor 47 and the data line 96, and the signal G to two of the subpixel electrodes 65 on the bottom substrate 30 by way of the branched data line 99. As in the previously described embodiments, the data voltages for the RGB subpixels are generated independently of one another by a separate driver chip which is TAB bonded to the panel. The TFT's and alignment layers are again not shown in Figures 19 and 20. It will be appreciated that, in this case, the number of the data connecting lines is decreased by 50% by comparison with the

embodiment of Figures 4 and 5. Again the use of the anisotropic conductor 47 avoids the need for an additional data line driver circuit for the subpixels controlling the reflected colour in both layers, but the technique again sacrifices some of the accessible colour space.

In one embodiment which works in a normally black (NB) mode the data voltage for a primary colour to be applied to two juxtaposed subpixels exhibiting absorption of this primary colour, so that, for example, the data voltage is applied to the centre and right subpixels on the bottom substrate 30 to modify the red reflectivity. In an alternative embodiment working in the normally white (NW) mode, the panel is driven in substantially the same manner as for the NB mode. In this case the controller comprises a different look-up table to modify the data output voltage according to the required grey level for each pair of subpixel electrodes. Thus, for example, the data voltage is applied to the centre and right subpixels on the bottom substrate 30 to modify the red reflectivity.

Figure 21 is a diagram, similar to that of Figure 11, but showing the signals for two pixels, each having six subpixels, supplied by way of the capacitative storage elements 81, 82 and the line buffers 83 to the substrates 20, 30 in the arrangements of Figures 13 to 16 and Figures 17 to 20. In this case two green (G) signals and two blue (B) signals are applied to the top substrate 20 and two red (R) signals and two blue signals are applied to the bottom substrate 30. The red, green and blue subpixels of each pixel as a whole are controlled in pairs by the appropriate data voltages.

Figure 22 is a schematic diagram, similar to that of Figure 4, of a further embodiment having a top active matrix substrate 20, a bottom active matrix substrate 30 and a conductive divider 21 interposed between the top and bottom substrates 20,30, and incorporating a scan line driver circuit 103 connected to the panel by N scan lines 102 and a data line driver circuit 45 connected to the panel by 2 x 3 M data lines 44. This embodiment is similar to the embodiment of Figures 4 and 5 except that the number of scan lines 102 is reduced by half by virtue of the fact that the same scan

signal is supplied to the juxtaposed scan lines of the top and bottom substrates 20, 30 using the same HSYNC signal, the scan lines of the top substrate 20 being connected by the conductor 46 to the scan lines of the bottom substrate 30 and the data lines of the top substrate 20 being connected by the conductor 47 to the data lines of the bottom substrate 30. The conductors 46 and 47 may be of the same form as described above with reference to any of the previously described embodiments.

Various modifications of the above described embodiments are possible within the scope of the invention. For example, instead of the AMLCD having two liquid crystal layers, the AMLCD may have three liquid crystal layers incorporating one or more liquid crystal mixtures and at least one anisotropic conductor for transferring scan and/or data signals from at least one substrate to at least one other substrate. The anisotropic conductor may be of different thicknesses and can also function as a sealing strip in the panel. In a further variant the driver circuitry may be fabricated on one of the substrates (system on panel) provided that the substrate is made from semiconducting material of sufficient mobility. This greatly reduces the required number of edge connections, thus reducing the need for short pitch connecting lines.

Furthermore Figure 23 is a schematic representation of an embodiment in which the scan line driver circuit 106 and the data line driver circuit 107 are integrally fabricated on the top, transmissive substrate 20 using polycrystalline TFT's on glass. For the purposes of illustration only the top and bottom substrates 20 and 30 are shown side by side, and the conductors 46 and 47 for transfer of scan and data voltages to the bottom, reflective substrate 30 are shown schematically. The scan lines of the top substrate 20 are connected to the scan lines of the bottom substrate 30 by the conductor 46, and the data lines of the top substrate 20 are connected to the data lines of the bottom substrate 30 by the conductor 47. The conductors 46 and 47 may be of the same form as described above with reference to any of the previously described embodiments.

Figure 24 shows a further embodiment in which separate scan line driver circuits 108 and 109 are provided on the top and bottom substrates 20 and 30, the top substrate

20 incorporating both scan line and data line driver circuits 107 and 108 and the bottom substrate 30 incorporating only the scan line driver circuit 109. For the purposes of illustration only the top and bottom substrates 20 and 30 are shown side by side. In this case the data lines of the top substrate 20 are connected to the data lines of the bottom substrate 30 by the conductor 47, which may be of any of the forms previously described. A further, non-illustrated embodiment is similar to the embodiment of Figure 23 except that the scan line driver circuit for the bottom, reflective substrate 30 is provided in a separate chip.

CLAIMS:

1. A multilayer display panel comprising a first layer incorporating a first matrix of display elements disposed at the intersections of first data lines and first scan lines, a second layer incorporating a second matrix of display elements disposed at the intersections of second data lines and second scan lines and overlying the first layer so that the second matrix is in register with the first matrix, and addressing means for addressing the display elements of the first layer by the application of data signals to the first data lines and scan signals to the first scan lines and for addressing the display elements of the second layer by the application of data signals to the second data lines and scan signals to the second scan lines, wherein the addressing means incorporates common driver circuit means having first connecting terminals for supplying the first data signals and/or the first scan signals to an edge portion of the first layer and second connecting terminals for supplying the second data signals and/or the second scan signals to a corresponding edge portion of the second layer, and at least one conducting element interposed between said edge portions of the first and second layers for transmitting the first data signals and/or the first scan signals from the first connecting terminals to the first layer.

2. A panel according to claim 1, wherein the first and second connecting terminals are connected to said edge portion of the second layer which includes connecting lines for receiving the first data signals and/or first scan signals from the first connecting terminals and for transmitting said signals to the first layer by way of the conducting element.

3. A panel according to claim 1 or 2, wherein the driver circuit means comprises a common data line driver circuit disposed in the vicinity of an edge of the panel for supplying the first and second data signals to the first and second layers.

4. A panel according to claim 3, wherein the data line driver circuit is fabricated on a common substrate with the first or second matrix.

5. A panel according to claim 3 or 4, wherein the driver circuit means further comprises separate scan line driver circuits disposed in the vicinity of an edge of the panel for supplying the first and second scan signals to the first and second layers.

6. A panel according to any one of claims 1 to 4, wherein the driver circuit means comprises a common scan line driver circuit disposed in the vicinity of an edge of the panel for supplying the first and second scan signals to the first and second layers.

7. A panel according to claim 6, wherein the scan line driver circuit is fabricated on a common substrate with the first matrix or the second matrix.

8. A panel according to any preceding claim, wherein the conducting element is an anisotropic conductor which is electrically conductive in a direction extending transversely to the first and second layers.

9. A panel according to any preceding claim, wherein the conducting element is constituted by an adhesive conductive strip interposed between said edge portions of the first and second layers.

10. A panel according to any preceding claim, wherein the display elements of the first and second layers are colour display elements comprising subelements at the intersections of corresponding data and scan lines for controlling display of a colour image in response to receipt of colour data signals by the subelements.

11. A panel according to claim 10, wherein the driver circuit means is arranged to supply three colour data signals to each display element of the first and second layers for the control of three colour components by the application of said signals to respective subelements of each display element.

12. A panel according to claim 10, wherein the driver circuit means is arranged to supply first and second colour data signals to each display element of the first layer and second and third colour data signals to each display element of the second layer.

13. A panel according to claim 12, wherein the first connecting terminals of the driver circuit means comprise respective connecting terminals for supplying the first and second colour data signals to the first layer, and the second connecting terminals of the driver circuit means comprise respective connecting terminals for supplying the second and third colour data signals to the second layer.

14. A panel according to claim 12, wherein the first and second connecting terminals of the driver circuit means comprise respective connecting terminals for supplying the first and third colour data signals to the first and second layers, and the driver circuit means includes further connecting terminals for supplying common second colour data signals to both the first layer and the second layer.

15. A panel according to my preceding claim, wherein the driver circuit means includes further connecting terminals for supplying common scan signals to both the first layer and the second layer.

16. A panel according to any preceding claim, which is a liquid crystal display panel.

17. A panel according to claim 16, which is an active matrix liquid crystal display panel.

The Patent Office

20

Application No: GB 9726087.1
Claims searched: 1-17

Examiner: Andrew Bartlett
Date of search: 21 April 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): G5C (CHB)

Int Cl (Ed.6): G02F 1/1347; G09G 3/36

Other: Online:- WPI, INSPEC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2062927 A	(CITIZEN WATCH CO.) See p5 line 4 et seq.	1-3,16 & 17 at least
A	US 5164853	(SHIMAZAKI) See fig 4 for example	1 at least
A	WO 97/32296 A1	(MOTOROLA) Se whole doc.	1 at least

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☒ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.